2M Async Fast SRAM

CS18FS2048(3/5/W)
CS16FS2048(3/5/W)

Revision History

Rev. No.	History	Issue Date
1.0	Initial issue	Apr..15,2014

GENERAL DESCRIPTION

The CS16FS2048(3/5/W) and CS18FS2048(3/5/W) are a 2,097,152-bit high-speed Static Random Access Memory organized as 128K(256) words by 16(8) bits. The CS16FS2048(3/5/W) (CS18FS2048(3/5/W)) uses 16(8) common input and output lines and have an output enable pin which operates faster than address access time at read cycle, And CS16FS2048(3/5/W) allows that lower and upper byte access by data byte control($\overline{UB}$, $\overline{LB}$).The device is fabricated using advanced CMOS process,6-TR based cell technology and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The CS16FS2048(3/5/W) is packaged in a 400mil 44-pin TSOP2 and 48FBGA. The CS18FS2048(3/5/W) is packaged in a 400mil 44-pin TSOP2 and 36FBGA.

FEATURES

- Fast Access Time 8,10,12,15ns(Max)
- CMOS Low Power Dissipation
  Standby (TTL): 10mA (Max.)
  (CMOS): 6mA (Max.)
  Operating: 35mA (8ns, Max..)
  : 30mA(10ns ,Max.)
- Single 3.3±0.3V or 5.0±0.5V Power Supply
- Wide range (1.65V~3.6V) of Power Supply
- TTL Compatible inputs and Outputs
- Fully Static Operation, No Clock or Refresh required
- Three State Outputs
- Data Byte Control(x16 Mode)
  $\overline{LB}$: I/O_0~I/O_7, $\overline{UB}$: I/O_8~I/O_{15}
- Standard 44TSOP2 and 36FBGA Package Pin Configuration for 256k x 8
- Standard 44TSOP2 and 48FBGA Package Pin Configuration for 128k x 16
- Operating in Commercial and Industrial Temperature range.

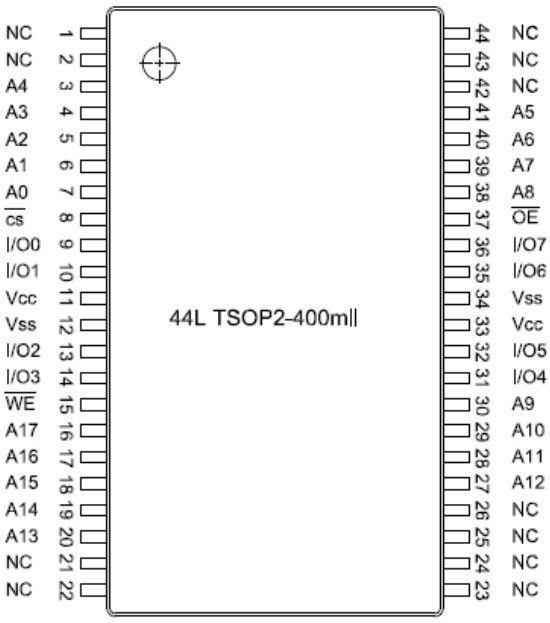
Order Information

Density	Org.	Part Number	V_{CC} (V)	Speed		Package	Temp.
				t_{AA}(ns)	t_{OE}(ns)		
2Mb	128Kx16	CS16FS20483GC(I)-08	3.3	8	4	44 TSOP2	C : Commercial I : Industrial
		CS16FS2048WGC(I)-08	3.3	8	4	44 TSOP2	
		CS16FS2048WGC(I)-10	2.5	10	5	44 TSOP2	
		CS16FS2048WGC(I)-12	1.8	12	6	44 TSOP2	
		CS16FS20483HC(I)-08	3.3	8	4	48 FBGA	
		CS16FS2048WHC(I)-08	3.3	8	4	48 FBGA	
		CS16FS2048WHC(I)-10	2.5	10	5	48 FBGA	
		CS16FS2048WHC(I)-12	1.8	12	6	48 FBGA	
		CS16FS20485GC(I)-10	5	10	5	44 TSOP2	
		CS16FS20483GC(I)-10	3.3	10	5	44 TSOP2	
		CS16FS2048WGC(I)-10	3.3	10	5	44 TSOP2	
		CS16FS2048WGC(I)-10	2.5	10	5	44 TSOP2	
		CS16FS2048WGC(I)-15	1.8	15	7	44 TSOP2	
		CS16FS20483HC(I)-10	3.3	10	5	48 FBGA	
		CS16FS2048WHC(I)-10	3.3	10	5	48 FBGA	
		CS16FS2048WHC(I)-10	2.5	10	5	48 FBGA	
		CS16FS2048WHC(I)-15	1.8	15	7	48 FBGA	

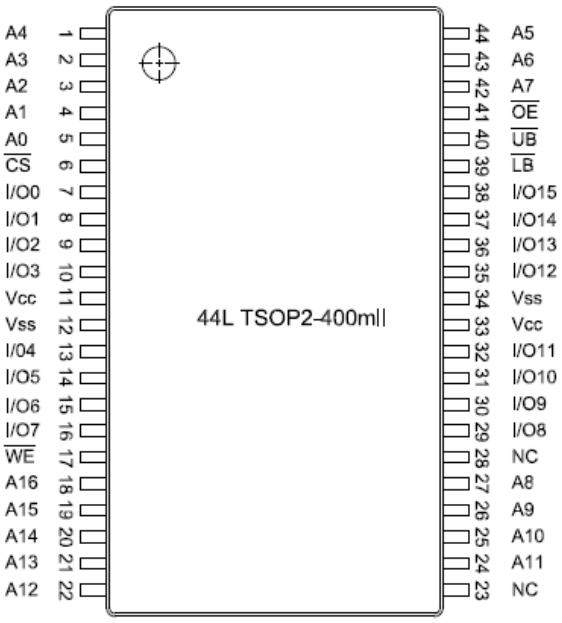
Density	Org.	Part Number	V_{CC}(V)	Speed		Package	Temp.
				t_{AA}(ns)	t_{OE}(ns)		
2Mb	256Kx8	CS18FS20483GC(I)-08	3.3	8	4	44 TSOP2	C : Commercial I : Industrial
		CS18FS2048WGC(I)-08	3.3	8	4	44 TSOP2	
		CS18FS2048WGC(I)-10	2.5	10	5	44 TSOP2	
		CS18FS2048WGC(I)-12	1.8	12	6	44 TSOP2	
		CS18FS20483YC(I)-08	3.3	8	4	36 FBGA	
		CS18FS2048WYC(I)-08	3.3	8	4	36 FBGA	
		CS18FS2048WYC(I)-10	2.5	10	5	36 FBGA	
		CS18FS2048WYC(I)-12	1.8	12	6	36 FBGA	
		CS18FS20485GC(I)-10	5	10	5	44 TSOP2	
		CS18FS20483GC(I)-10	3.3	10	5	44 TSOP2	
		CS18FS2048WGC(I)-10	3.3	10	5	44 TSOP2	
		CS18FS2048WGC(I)-10	2.5	10	5	44 TSOP2	
		CS18FS2048WGC(I)-15	1.8	15	7	44 TSOP2	
		CS18FS20483YC(I)-10	3.3	10	5	36 FBGA	
		CS18FS2048WYC(I)-10	3.3	10	5	36 FBGA	
		CS18FS2048WYC(I)-10	2.5	10	5	36 FBGA	
		CS18FS2048WYC(I)-15	1.8	15	7	36 FBGA	

PIN CONFIGURATIONS

44TSOP2-400mil



CS18FS2048(3/5/W)- (256k x 8)



CS16FS2048(3/5/W)- (128k x 16)

6x8mm mini-BGA with ball pitch 0.75mm

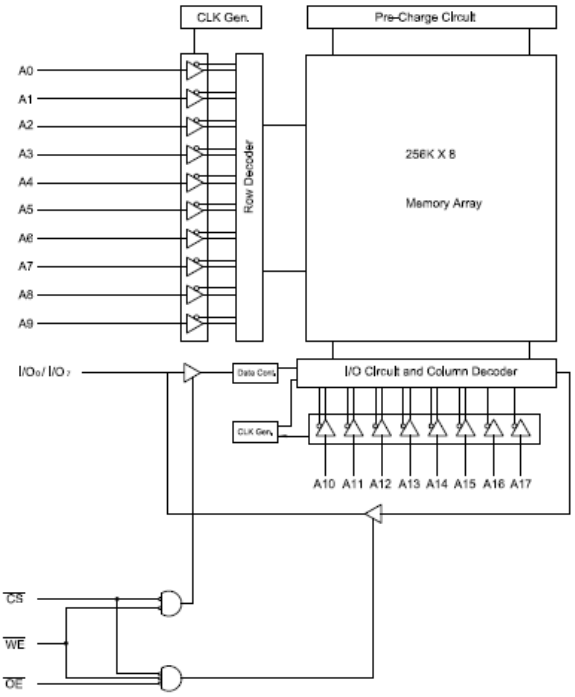
	1	2	3	4	5	6
A	A0	A1	NC	A3	A6	A8
B	IO4	A2	$\overline{WE}$	A4	A7	IO0
C	IO5		NC	A5		IO1
D	Vss					Vcc
E	Vcc					Vss
F	IO6		NC	A17		IO2
G	IO7	$\overline{OE}$	$\overline{CS}$	A16	A15	IO3
H	A9	A10	A11	A12	A13	A14

CS18FS2048(3/5/W) – (256k x 8)
36 ball mini-BGA

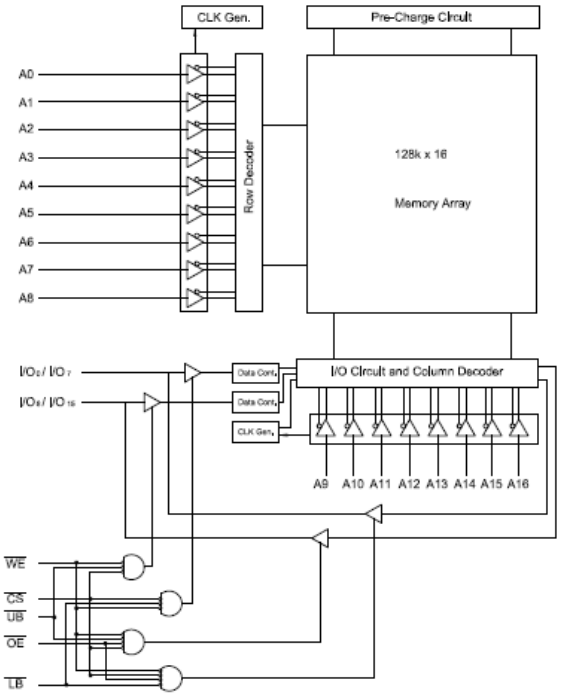
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	IO8	$\overline{UB}$	A3	A4	$\overline{CS}$	IO0
C	IO9	IO10	A5	A6	IO1	IO2
D	Vss	IO11	NC	A7	IO3	Vcc
E	Vcc	IO12	NC	A16	IO4	Vss
F	IO14	IO13	A14	A15	IO5	IO6
G	IO15	NC	A12	A13	$\overline{WE}$	IO7
H	NC	A8	A9	A10	A11	NC

CS16FS2048(3/5/W) – (128k x 16)
48ball mini-BGA

● FUNCTIONAL BLOCK DIAGRAM



CS18FS2048(3/5/W) – (256k x 8)



CS16FS2048(3/5/W) – (128k x 16)

Absolute Maximum Ratings*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	3.3V Product	V_{in}, V_{OUT}	-0.5 to V_{CC}+0.5V	V
	5.0V Product			
	Wide V_{CC}** Product			
Voltage on V_{CC} Supply Relative to V_{SS}	3.3V Product	V_{in}, V_{OUT}	-0.5 to 4.6	V
	5.0V Product		-0.5 to 7.0	
	Wide V_{CC}** Product		-0.5 to 4.6	
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature Commercial		T_A	0 to 70	°C
Industrial		T_A	-40 to 85	°C

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Wide VCC Range is 1.65V~3.6V

Recommended DC Operating Conditions*(T_A=0 to 70℃)

Parameter	Operating V_{CC}(V)	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	5.0	V_{CC}	4.5	5.0	5.5	V
	3.3	V_{CC}	3.0	3.3	3.6	
	Wide 2.4~3.6	V_{CC}	2.4	2.5/3.3	3.6	
	Wide 1.65~2.2	V_{CC}	1.65	1.8	2.2	
Ground		V_{SS}	0	0	0	V
Input High Voltage	5.0	V_{IH}	2.2	-	V_{CC}+0.5	V
	3.3	V_{IH}	2.0	-	V_{CC}+0.5	
	Wide 2.4~3.6	V_{IH}	2.0	-	V_{CC}+0.3	
	Wide 1.65~2.2	V_{IH}	1.4	-	V_{CC}+0.2	
Input Low Voltage	5.0	V_{IL}	-0.3	-	0.8	V
	3.3	V_{IL}	-0.3	-	0.8	
	Wide 2.4~3.6	V_{IL}	-0.3	-	0.7	
	Wide 1.65~2.2	V_{IL}	-0.2	-	0.4	

*The above parameters are also guaranteed for industrial temperature range.

DC and Operating Characteristics*(T_A=0 to 70℃)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}	-2	2	uA
Output	I_{LO}	$\overline{CS}$ =V_{IH} or $\overline{OE}$ =V_{IH} or $\overline{WE}$ = V_{IL}	-2	2	uA

Leakage Current**		V_{OUT}=V_{SS} to V_{CC}				
Operating Current**	I_{CC}	Min.Cycle,100% Duty $\overline{CS}$ =V_{IL}, V_{IN}=V_{IH} or V_{IL},I_{OUT}= 0mA	8ns	-	35	mA
			10ns		30	
			12ns	-	28	
			15ns		25	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$ =V_{IH}		-	10	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥V_{CC}-0.2V V_{IN}≥V_{CC}-0.2V or V_{in}≦0.2V		-	6	
Output Low Voltage Level	V_{OL}	V_{CC} =4.5V, I_{OL}=8mA, 5.0V Product		-	0.4	V
		V_{CC}=3.0V, I_{OL}=8mA, 3.3V Product & Wide V_{CC}** Product		-	0.4	
		V_{CC}=2.4V, I_{OL}=1mA, Wide V_{CC}** Product		-	0.4	
		V_{CC}=1.65V, I_{OL}=0.1mA, Wide V_{CC}** Product		-	0.2	
Output High Voltage Level	V_{OH}	V_{CC}=4.5V, I_{OH}= -4mA, 5.0V Product		2.4	-	V
		V_{CC}=3.0V, I_{OH}= -4mA, 3.3V Product & Wide V_{CC}** Product		2.4	-	
		V_{CC}=2.4V, I_{OH}= -1mA, Wide V_{CC}** Product		1.8	-	
		V_{CC}=1.65V, I_{OH}= -0.1mA, Wide V_{CC}** Product		1.4	-	

*The above parameters are also guarantee for industrial temperature range.

**Wide V_{CC} Range is 1.65V ~ 3.6V

Capacitance*(T_A= 25℃, f= 1.0MHz)

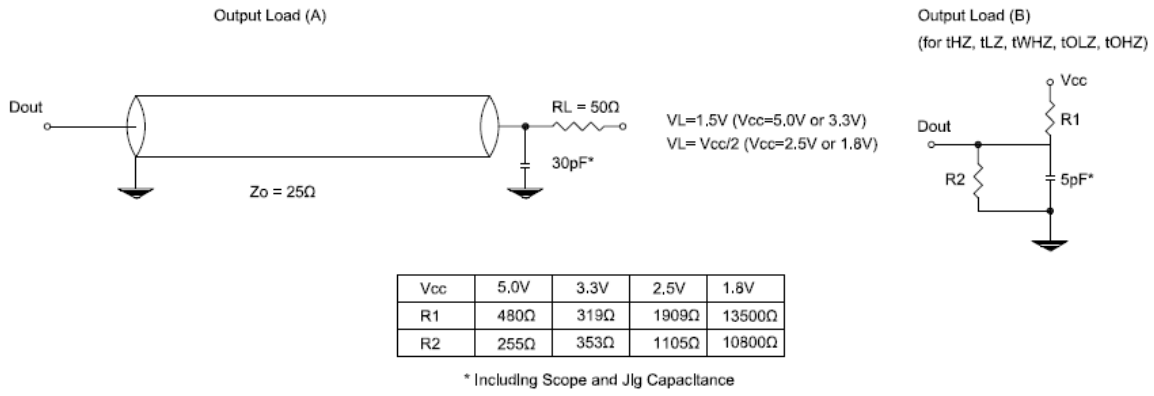
Item	Symbol	Test Conditions	TYP	Max	Unit
Input/ Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF

*Capacitance is sampled and not 100% tested.

Test Conditions*

Parameter	Value
Input/ Output Capacitance	0 to 3.0V (V_{CC}=3.3V or 5.0V)
	0 to 2.5V (V_{CC}=2.5V)
	0 to 1.8V (V_{CC}=1.8V)
Input Rise and Fall Time	1V/1ns
Input and Output Timing Reference Levels	1.5V (V_{CC}=3.3V or 5.0V)
	1/2V_{CC} (V_{CC}= 1.8V or 2.5V)
Output Load	See Fig. 1

*The above parameters are also guaranteed for industrial temperature range.



Vcc	5.0V	3.3V	2.5V	1.8V
R1	480Ω	319Ω	190Ω	13500Ω
R2	255Ω	353Ω	1105Ω	10800Ω

* Including Scope and Jig Capacitance

Fig 1

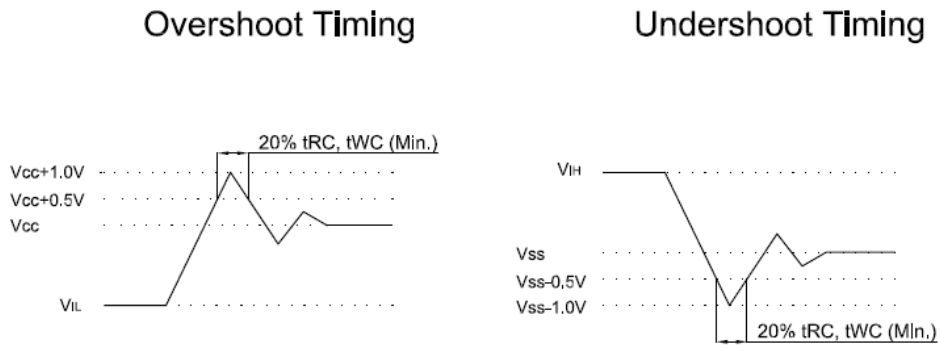


Fig 2

Functional Description (x8 Mode)

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB},I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

*X means don't care

Functional Description (x16 Mode)

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$ **	$\overline{UB}$ **	Mode	I/O Pin		Supply Current
						I/O_0~I/O_7	I/O_8~I/O_{15}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

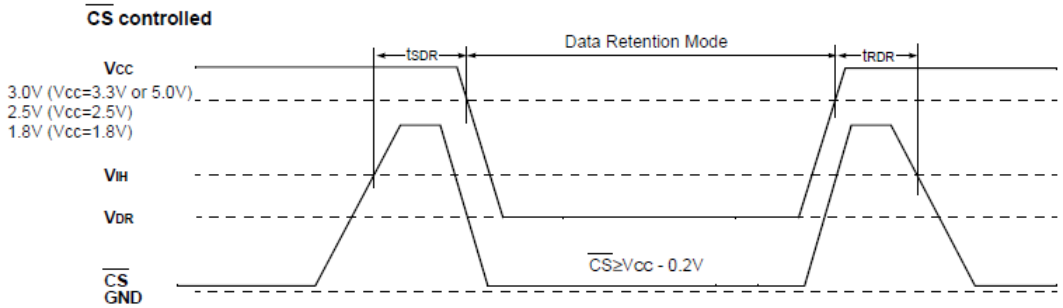
*X means don't care

Data Retention Characteristics*(T_A=0 to 70℃)

Parameter	Product	Operating V_{CC}(V)	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	5.0V Product	5.0	V_{DR}	$\overline{CS}$ ≥V_{CC} - 0.2V	2.0	-	5.5	V
	3.3V Product	3.3			2.0	-	3.6	
	Wide 2.4V~3.6V	2.5/3.3			2.0	-	3.6	

	Wide 1.65V~2.2V	1.8			1.5	-	3.6	
Data Retention Current	5.0V Product	5.0	I_{DR}	V_{CC}=2.0V $\overline{CS}$ ≥V_{CC} - 0.2V V_{IN}≥ V_{CC} - 0.2V or V_{IN}≤0.2V	-	-	5	mA
	3.3V Product	3.3			-	-	5	
	Wide 2.4V~3.6V	2.5/3.3			-	-	6	
	Wide 1.65V~2.2V	1.8		V_{CC}=1.5V, $\overline{CS}$ ≥V_{CC} - 0.2V, V_{IN}≥V_{CC}- 0.2V or V_{IN}≤0.2V	-	-	6	
Data Retention Set-Up Time			t_{SDR}	See Data Retention Wave form (below)	0	-	-	nS
Recovery Time			t_{RDR}		5	-	-	mS

Data Retention Wave form



Read Cycle*

Parameter	Symbol	8ns		10ns		12ns		15ns		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	-	15	ns
Chip Select to Output	t_{CO}	-	8	-	10	-	12	-	15	ns
Output Enable to Valid Output	t_{OE}	-	4	-	5	-	6	-	7	ns

$\overline{UB}$, $\overline{LB}$ Access Time**	t_{BA}	-	4	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output**	t_{BLZ}	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	5	0	6	0	7	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	0	6	0	7	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output**	t_{BHZ}	0	4	0	5	0	6	0	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection Power Up Time	t_{PU}	0	-	0	-	0	-	0	-	ns
Chip Selection Power Down Time	t_{PD}	-	8	-	10	-	12	-	15	ns

*The above parameters are also guaranteed for industrial temperature range.

Write Cycle*

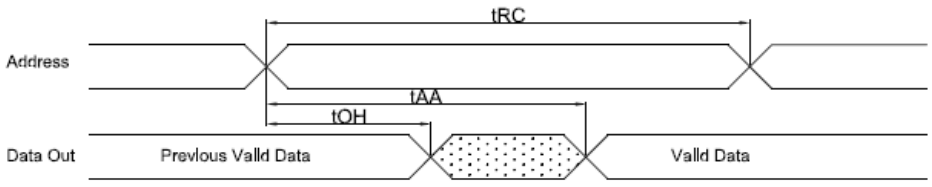
Parameter	Symbol	8ns		10ns		12ns		15ns		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	15	-	ns
Chip Select to End of Write	t_{CW}	6	-	7	-	9	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	6	-	7	-	9	-	12	-	ns

Write Pulse Width($\overline{OE}$ High)	t_{WP}	6	-	7	-	9	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP1}	8	-	10	-	12	-	15	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write**	t_{BW}	6	-	7	-	9	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	0	4	0	5	0	6	0	7	ns
Data to Write Time Overlap	t_{DW}	4	-	5	-	7		8	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
End of Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	3	-	ns

*The above parameters are also guaranteed for industrial temperature range.

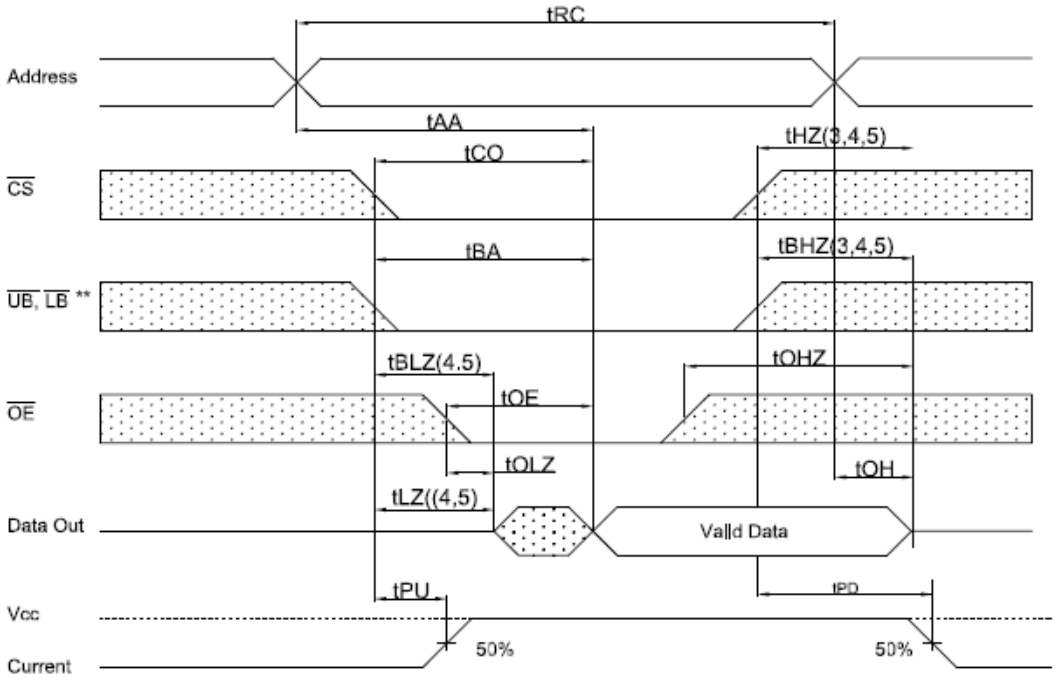
Timing Diagram

Timing Waveform of Read Cycle (1) (Address Controlled, $\overline{CS}$ = $\overline{OE}$ =V_{IL}, $\overline{WE}$ =V_{IH}, $\overline{UB}$, $\overline{LB}$ =V_{IL} **)



** Those parameters are applied for x16 mode only.

Timing Waveform of Read Cycle (2) ($\overline{WE}$ =VIH)

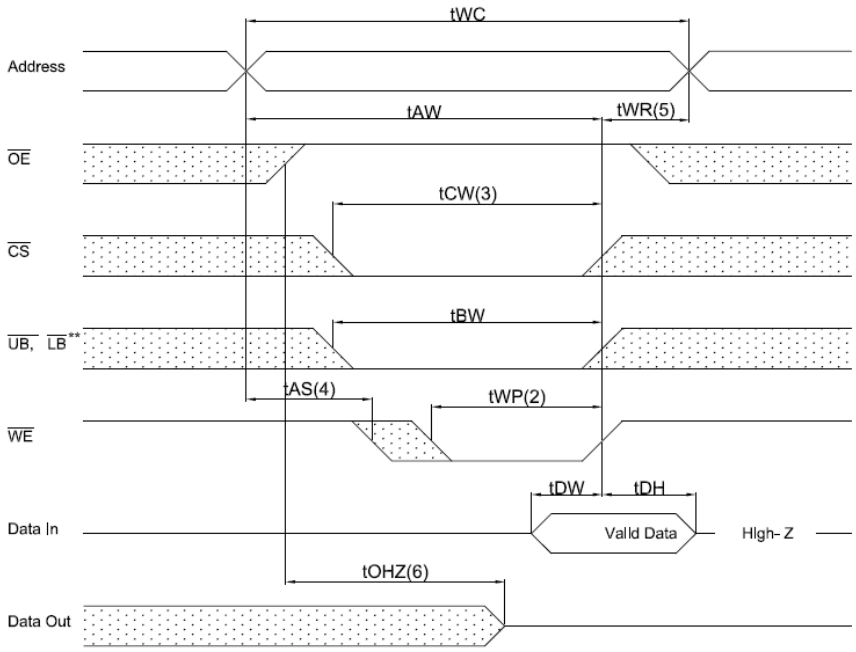


NOTES (Read Cycle)

1. $\overline{WE}$ is high for read cycle
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ} (Max.) is less than t_{LZ} (Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

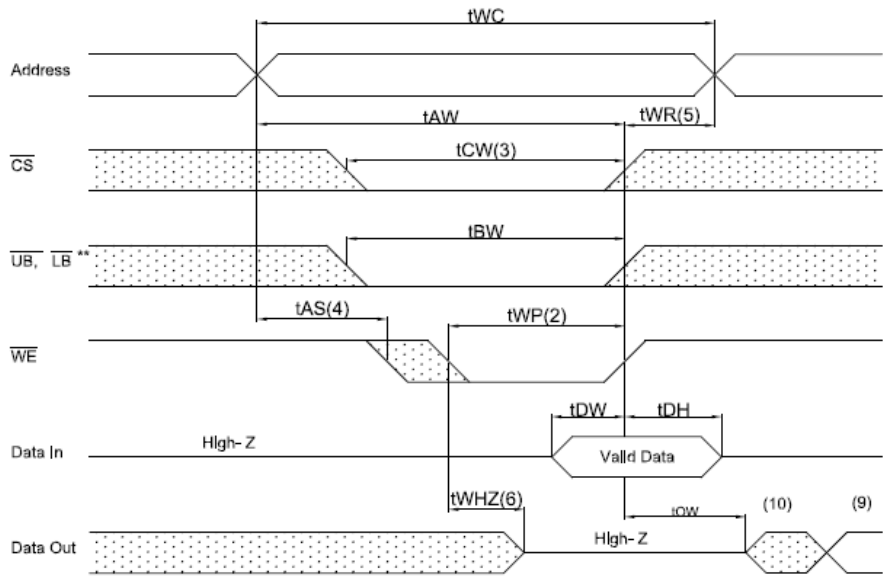
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle (1) ($\overline{OE}$ Clock)



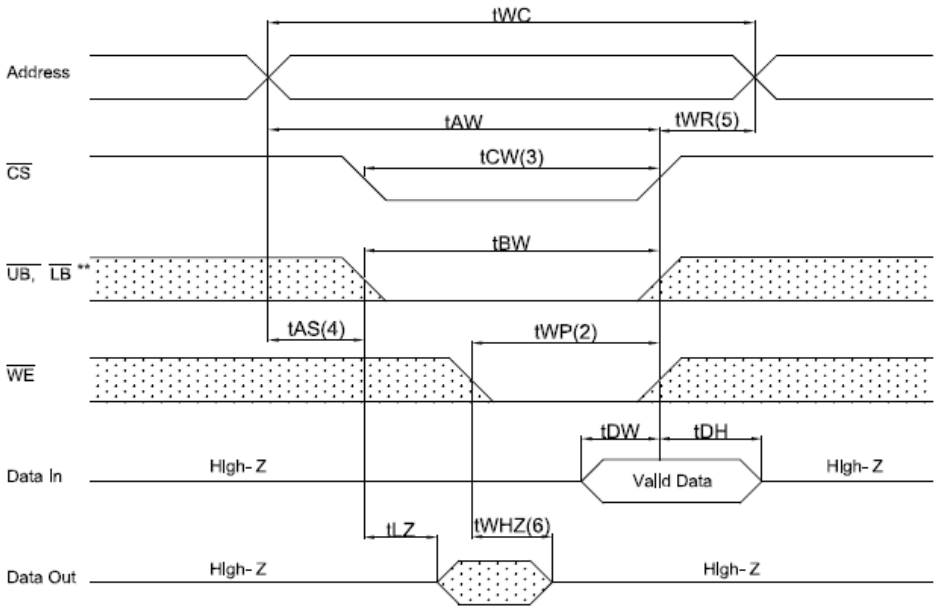
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle (2) ($\overline{OE}$ =Low fixed)



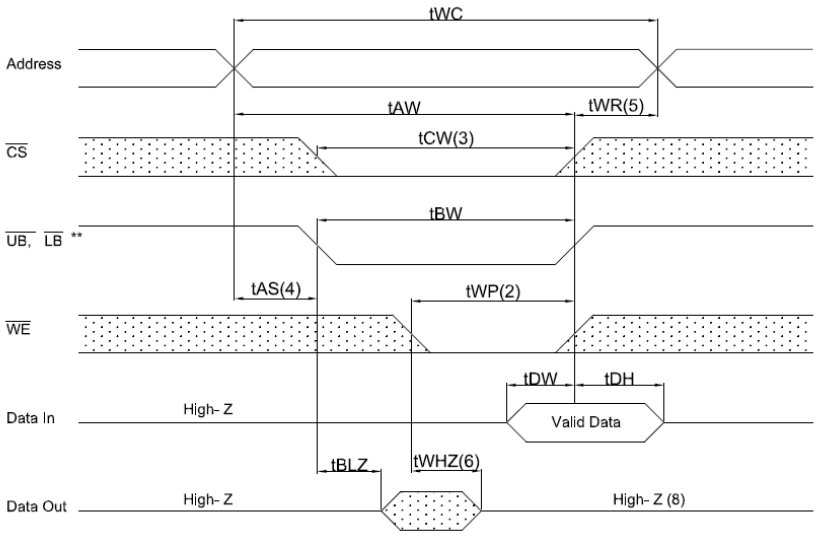
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle (3) ($\overline{CS}$ =Controlled)



** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle (4) ($\overline{UB}$, $\overline{LB}$ Controlled)



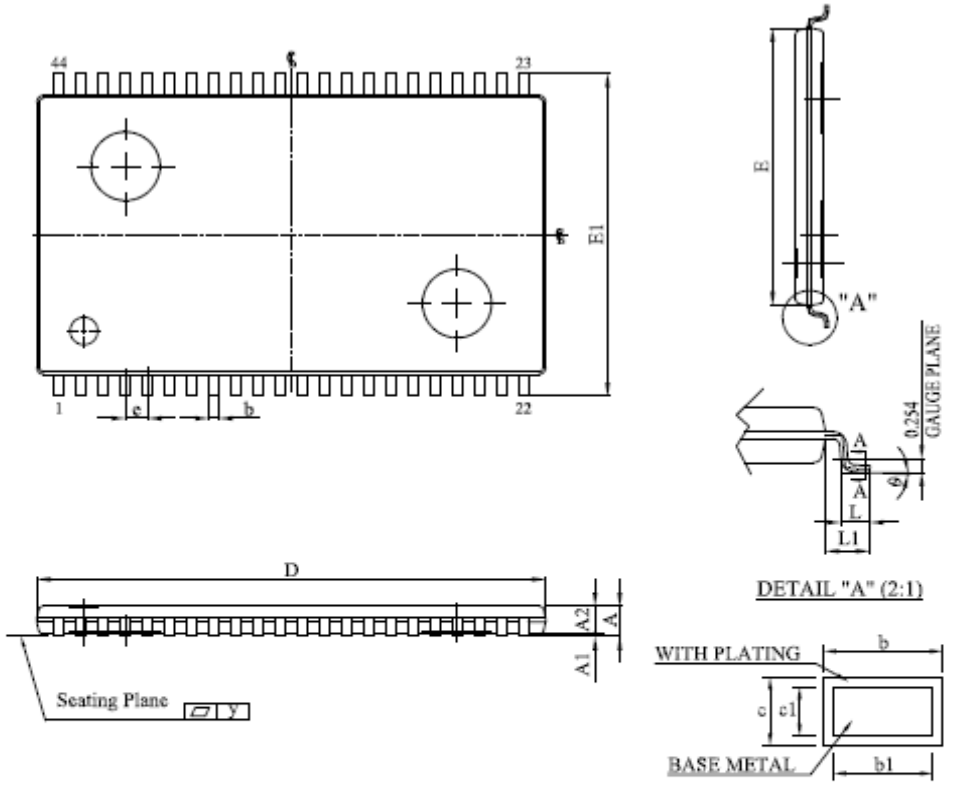
NOTES (Write Cycle)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ;
   A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. $\overline{WE}$ is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after WE going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

** Those parameters are applied for x16 mode only

Package outline dimensions

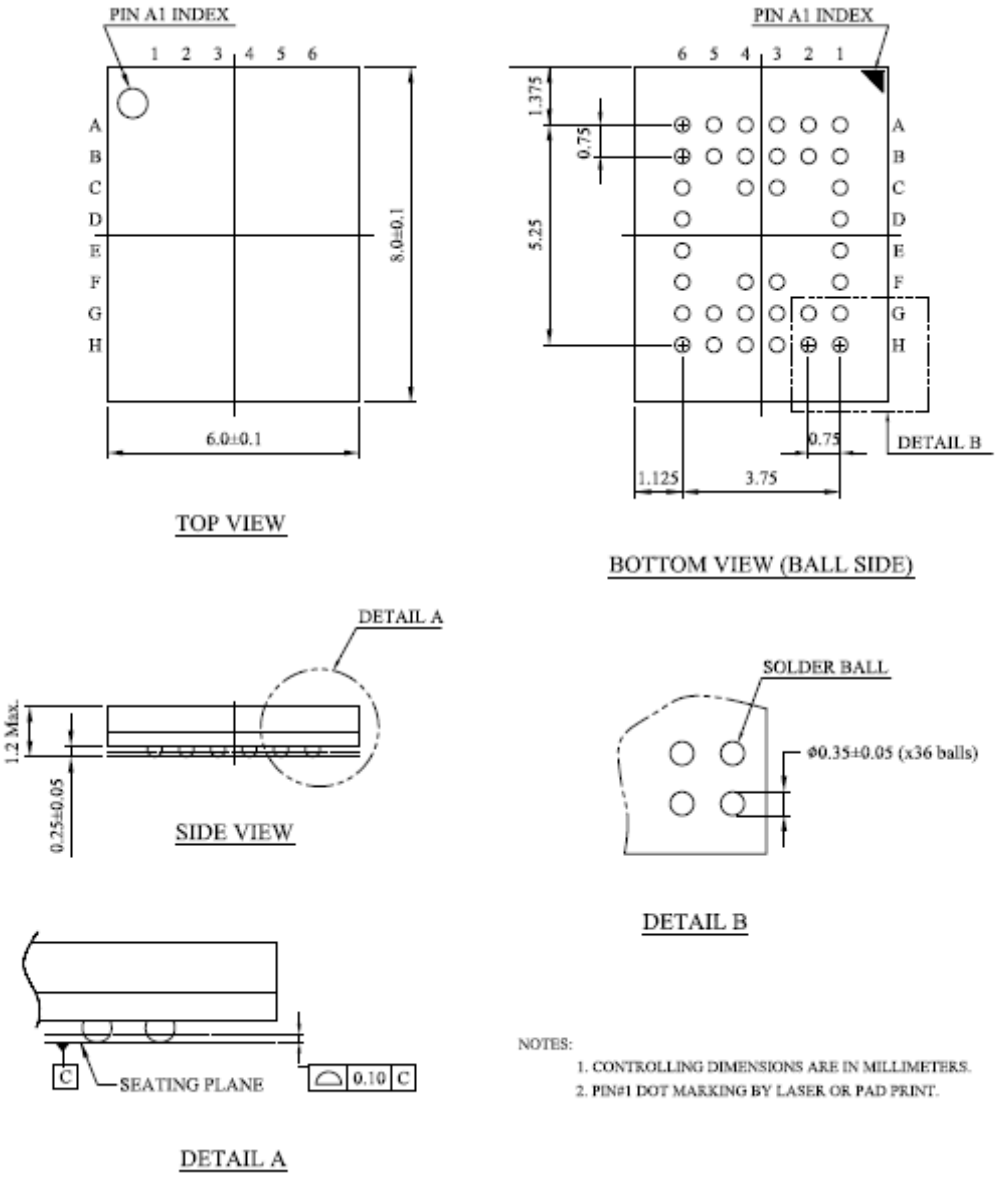
44L-TSOP2-400mil



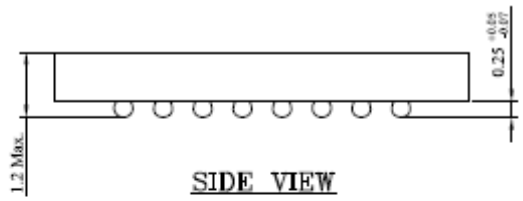
Note: Plating thickness spec : 0.3 mil – 0.8 mil.

SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	θ
mm	Min.	1.00	0.05	0.95	0.30	0.30	0.12	0.12	18.31	10.06	11.56	0.70	0.40	0.70	–	0°
	Nom.	1.10	0.10	1.00	–	–	–	–	18.41	10.16	11.76	0.80	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.45	0.40	0.21	0.16	18.51	10.26	11.96	0.90	0.60	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.012	0.012	0.005	0.005	0.721	0.396	0.455	0.0275	0.0157	0.0275	–	0°
	Nom.	0.0433	0.004	0.039	–	–	–	–	0.725	0.400	0.463	0.0315	0.0197	0.0315	–	–
	Max.	0.0473	0.006	0.041	0.018	0.016	0.008	0.006	0.729	0.404	0.471	0.0355	0.0237	0.0355	0.004	8°

36ball mini-BGA-6x8mm (ball pitch: 0.75mm)

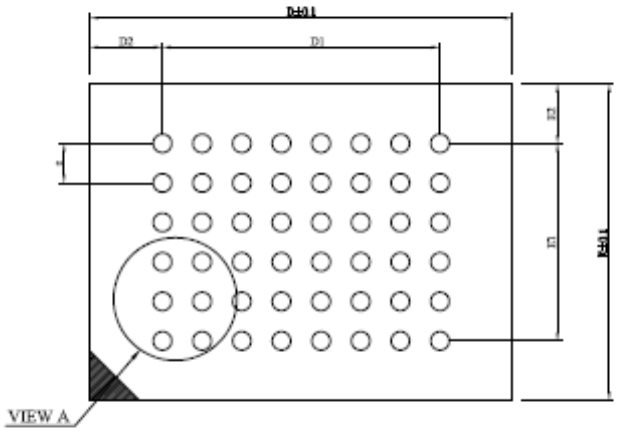


48ball mini-BGA-6x8mm (ball pitch: 0.75mm)

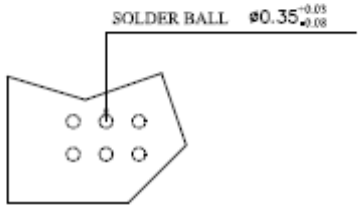


SIDE VIEW

BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125



TOP VIEW



VIEW A

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:
   LINEAR : X.X = ±0.1
   X.XX = ± 0.05
   X.XXX = ± 0.025